Semiconductor and Materials Division

XEROX

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PRODUCTION ENGINEERING MEASURE
ON
300 WATT SILICON AUDIO TRANSISTOR

Contract No. DA-36-039-SC-85968

for

Production Development Division
Division for Industrial Mobilization
The Army Signal Supply Agency
Philadelphia, Pennsylvania

PERIOD COVERED:

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Symbol	Explanation
BV_{CBO}	Breakdown Voltage, Collector-to-Base, emitter open
BV_{EBO}	Breakdown Voltage, Emitter-to-Base, collector open
C_{ob}	Output Capacitance, common base
f_{max}	Maximum Frequency of Oscillation
I	Intrinsic or undiffused layer
I_C	Collector current, DC
I_{CBO}	Collector Cutoff Current, DC, emitter open
I_{CER}	Collector Cutoff Current, DC, with specified resistance between base and emitter
I_{EBO}	Emitter Cutoff Current, DC, collector open
$r_{bb'}$	Base Spreading Resistance
R_{BE}	External Base-to-Emitter Resistance
τ_{ec}	Maximum Allowable Transit Time, Minority Carrier, Emitter-to-Collector
τ_e	Emitter Phase Delay Time
τ_b	Base Transit Time
τ_c	Collector Transit Time
V_{CBO}	Collector-to-Base Voltage, DC, emitter open
V_{CEO}	Collector-to-Emitter Voltage, DC, base open
V_{CER}	Collector-to-Emitter Voltage, DC, with specified resistance between emitter and base
$\frac{kt}{q}$	Constant equal to 0.026 volts
h_{FE}	Static value of the forward current transfer ratio (common emitter)
V_{CE} (sat)	Collector-to-Emitter Saturation Voltage
n	Efficiency
θ	Thermal Resistance

ABSTRACT

This abstract gives a brief description of the significant accomplishments of Signal Corps Three-Hundred Watt Audio Transistor Program DA-36-039-SC-85968 by the Radio Corporation of America (Semiconductor and Materials Division) during the period from June 21, 1961 to September 30, 1961.

A triple-diffused, NPIN transistor has been selected as the device for fabrication as the specified three-hundred watt, audio transistor. This type of structure will permit the desired characteristics of reduced base resistance, minimized collector-to-emitter punch-through voltage, high collector breakdown voltages, small base widths without reaching a punch-through condition, and good current gains. Calculations have been made of the collector breakdown voltage, current gain, thermal resistance, power gain, and power dissipation, and with a few reservations, the present device geometry should satisfy the contract specifications. A new case, a double-ended stud package, has been designed, and parts ordered.

The tentative Process Flow Chart for the device fabrication is as follows:

> Wafer Preparation; Multiple Collector Formation; Multiple Emitter Formation; Multiple Contacting; Multiple Mesa Formation; Pellet Separation; Individual Device Mounting and Sealing; and Individual Device Evaluation.

In the mounting and sealing area, some work has been done to use a molybdenum platform, 0.050" thick, between the pellet and the header. This particular thickness prevents problems with warping in subsequent fabrication processes. A change in the type of material used to contact the mesa has been made. Gold ribbon is now used in place of the previously used gold wire because of the increased current-handling capabilities possible.

Five state-of-the-art samples of the device have already been given to Mr. C. Fisher of the Signal Corps on September 22, 1961, and the electrical characteristics are presented.

The biographies of the personnel contributing directly to this program are presented and the Man Hours for this quarter and to-date are included.

I. PURPOSE

The purpose of this contract is to establish an industrial capability to manufacture a 300 watt silicon transistor. This capability will be demonstrated by operating a pilot line, containing the necessary prototype (where applicable) equipment to fabricate this device, capable of a production rate of at least 200 transistors, conforming to the applicable specifications (MIL-S-19500B, SCS-100 etc.), per eight (8) hour shift day. Furthermore, a total of 175 samples must be submitted to the Contracting Agency, together with all required reports. In addition, 1000 transistors from the pilot line conforming to the applicable specifications will be submitted.

II. DEVICE DESIGN CONSIDERATIONS

A. General

The design selected as the one for the TA-2167 (subject contract device) is a triple-diffused, NPIN structure. An NPIN transistor differs from a conventional NPN transistor in that it has a high resistivity layer in the collector body. In an NPN structure, the collector-to-base breakdown voltage is dependent primarily upon the impurity gradient in the base and the background resistivity of the collector. A shallow impurity gradient in the base is therefore necessary to obtain a high collector-to-base breakdown voltage. In an intrinsic layer device, the collector breakdown voltage is dependent primarily on the width of the intrinsic layer. The depletion region will extend primarily into the collector body thereby reducing the field strength at a given reverse voltage. Therefore, a highly doped base region can be used in an NPIN device to reduce base resistance and minimize collector-to-emitter punch-through voltage while simultaneously permitting high collector breakdown voltages. The base widths can be made extremely small without reaching a punch-through condition, and good current gains can be achieved.

The first consideration in the design of this device is to obtain the required 300 volt collector-breakdown voltage both in the open-emitter and open-base configurations.

B. Collector Breakdown Voltage

The theoretical breakdown field for 20-40 ohm-cm silicon is about 3×10^5 volts/cm or 750 volts/mil. However, experience has shown that because of variations in the intrinsic layer width (caused by uneven impurity penetrations and lapping) a wider intrinsic layer than estimated by this figure should

be used. In practice, a 2.0 mil intrinsic layer will result in an 800 volt collector breakdown in the open-emitter circuit configuration.

The collector-to-emitter, open-base voltage (V_{CEO}) can be estimated from the following relationship:

$$V_{CEO} = \frac{V_{CBO}}{\sqrt[n]{h_{fe} + 1}} \quad \ldots\ldots\ldots\ldots\ldots (1)$$

For this device, the empirically derived a lanche multiplication factor(n) has a value of 9. For units having a current gain of 50, and still meeting the 300 volt V_{CEO} requirement, a V_{CBO} of 550 volts is required. Therefore, a 2 mil intrinsic layer will provide a transistor that will meet the contract collector specification.

C. Current Gain

At sufficiently high current levels all transistors show a fall-off of current gain with current. The specification for this device requires a current gain of 15-45 at a collector current of five amperes, and 10 at a collector current of ten amperes.

Previous investigations conducted have shown that, at high current densities, a transverse voltage developed in the base layer causes carrier injection to be confined primarily to the edges of the emitter. Therefore, the emitter peripheral distance, rather than the emitter area, is the significant parameter in the design consideration. Experience has shown that current gain will peak at a current density of approximately one ma/mil of emitter periphery. Originally, an emitter periphery of five inches was thought to be necessary, but recent data indicate that 2.2 inches of emitter periphery are adequate.

D. Thermal Resistance

The maximum junction to case thermal resistance of the TA-2167 is 0.58 °C/watt. This value is determined by the specified values of 300 watts power dissipation, 200 °C maximum junction temperature, and 25°C case temperature and can be calculated according to the following equation:

$$\Theta_{JC} = \frac{T_J - T_C}{P_D} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

Assuming the transistor operates as an amplifier with 65% efficiency, the power to be dissipated by each transistor, when two units are operating in push-pull with a power output of 500 watts, can be determined from the following:

$$P_D = \left(\frac{1 - n}{n}\right) (P_O) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3)$$

This dissipation, when calculated, is 135 watts for each of the transistors. The maximum allowable case-to-ambient thermal resistance is 1.3 °C/watt when calculated from the following equation:

$$\Theta_{JA} = \frac{T_J - T_A}{P_D} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4)$$

Since the junction-to-case thermal resistance is 0.58 °C/watt, the maximum case-to-ambient thermal resistance is about 0.7 °C/watt. This low thermal resistance requirement will mean that the unit should be operated in a water-cooled heat sink when large amounts of power must be dissipated.

Some preliminary design work has been done in the area of Thermal Rating of the TA-2167. Theoretically this device is capable of dissipating 300 watts if the transistor case can be maintained at the ambient temperature of 25°C. As the ambient temperature increases, the corresponding

maximum transistor dissipation decreases. The rate of decrease in $P_{D\ max.}$ can be determined from the derating curve for the device. The negative slope of this curve represents the thermal resistance of the transistor. If the case temperature is to be maintained at the ambient temperature, any operating point along the derating curve would require an infinite heat sink.

In most silicon transistor applications the ambient temperature is considerably lower than that of the case. This temperature difference divided by the power dissipation determines the minimum case-to-ambient thermal resistance required to keep the junction temperature within the maximum rating of 200°C.

The case-to-ambient thermal resistance consists of the contact thermal resistance and the heat sink thermal resistance. A plot of the case-to-ambient thermal resistance (Θ_{CA}) versus T_C for various ambient temperatures is superimposed on the derating curve for the TA-2167 in Figure 1. This graph enables the designer to determine the minimum case-to-ambient thermal resistance necessary to prevent overheating the junction. Further work is continuing in this area.

E. Power Gain

The peak current of the TA-2167 can be calculated from the following equation:

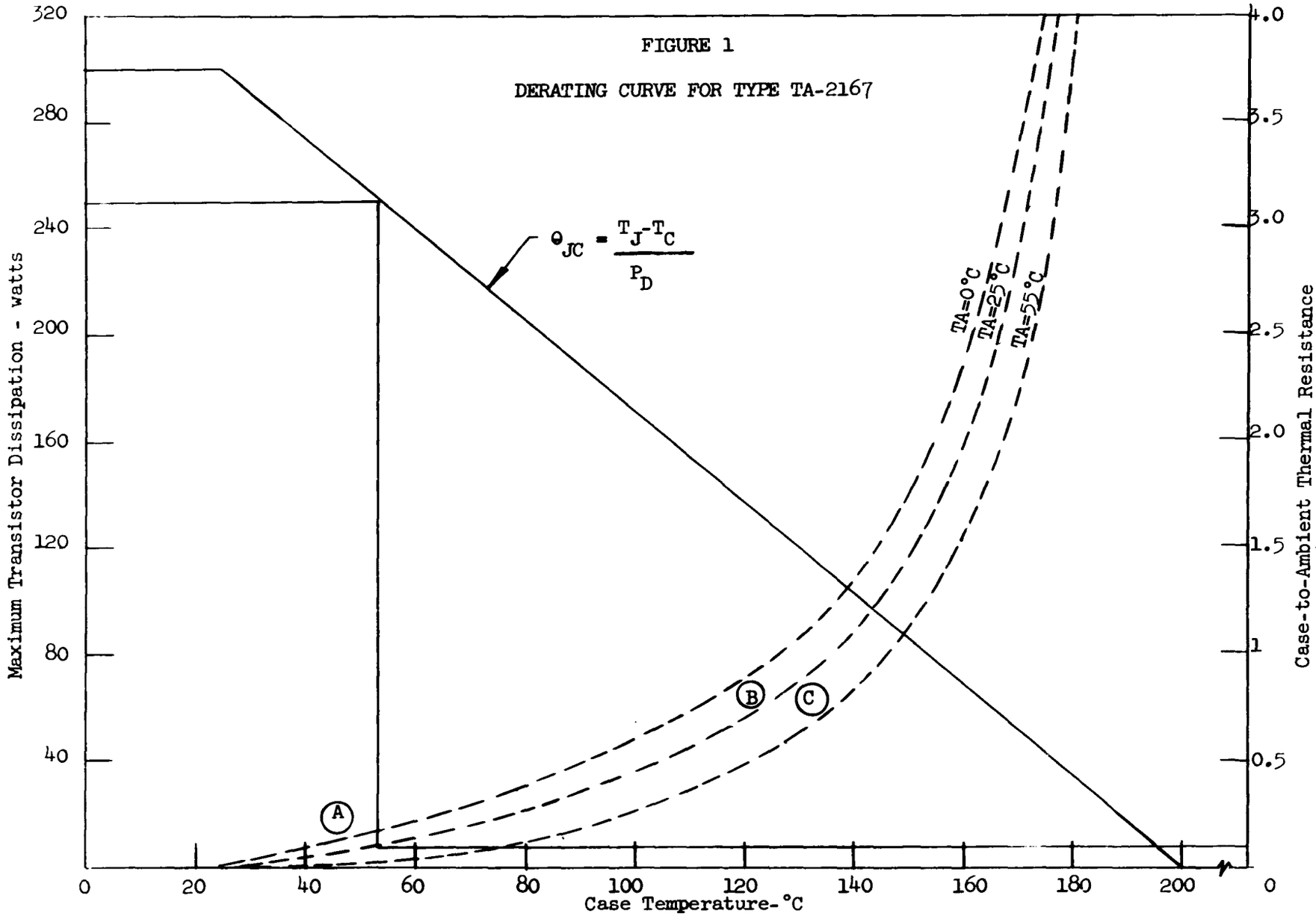
$$P_{AC} = \frac{I_P E_P}{4} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (5)$$

For an AC power of 250 watts per device operating at 120 volts, the peak current is 8.3 amperes. The load resistance for the transistor at this voltage and current level is then computed as follows:

$$R_L = \frac{E_P}{I_P} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (6)$$

FIGURE 1

DERATING CURVE FOR TYPE TA-2167



and is equal to 14.4 ohms. The power gain can then be estimated from the following equation:

$$P.G. = \beta^2 \frac{R_L}{R_{IN}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (7)$$

To obtain a minimum beta of ten and a power gain of twenty-five db, as specified in the technical requirements, the maximum input resistance is 4.6 ohms. No difficulty is anticipated in meeting this specification because the input resistance is expected to be about one ohm.

F. Case Design

A double-ended stud package has been designed for this device, and will be used to dissipate the heat required. A drawing of this package is shown in Figure 2. Sample parts have been received and are presently being evaluated. Delivery of reasonable quantities of this package for device fabrication are not due until late in October. At that time, use of the new case design should be incorporated into the standard processing of the TA-2167.

Initial device state-of-the-art samples will be enclosed in the single-ended stud packages shown in Figure 3, and delivered to the contracting agency.

G. Power Dissipation

A problem has occured in the high voltage testing of the TA-2167 device for this contract. This problem has been found to exist in other high power devices. A negative resistance effect occurs when the common-emitter configuration family of curves is examined on a curve tracer. This effect, which is called the "crossover voltage", occurs at what is called the "crossover point". This "crossover point" is at approximately 100 volts and one ampere of collector current. At this point there is a sudden increase in current as the voltage across the transistor decreases. Although this phenomenon is present in

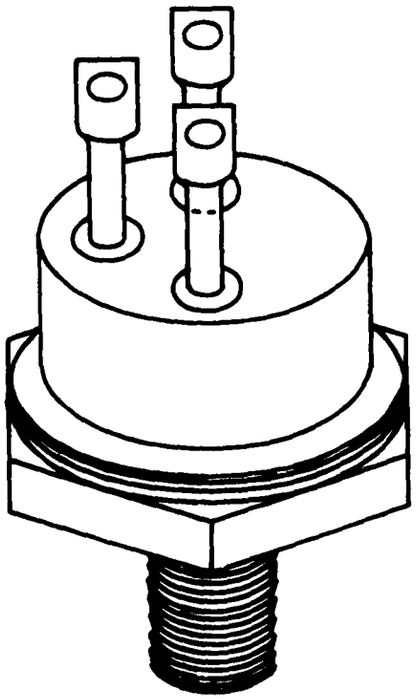


FIGURE 2

DOUBLE-ENDED STUD PACKAGE FOR THE TA-2167

FIGURE 3

PHOTOGRAPH OF SINGLE-ENDED STUD PACKAGES USED TO ENCLOSE INITIAL STATE-OF-THE-ART SAMPLES

most other transistor devices, it has not caused a problem there because the point occurs outside the rated operating range.

It has been found that, if the transistor is used in a circuit which provides 100 microsecond pulses, the transistor is easily able to handle a current of ten amperes and show no "crossover voltage" even at a voltage level of 300 volts. Because of this investigation, the device evaluation will be based on circuit performance rather than on a dynamic display of the device characteristics until the crossover problem is solved.

Further design work is being done in an attempt to solve this problem.

III. DEVICE FABRICATION

A. Parts and Materials

A flow chart of the major parts and materials used to fabricate the TA-2167 transistor is shown in Figure 4. As detailed engineering drawings and specifications for the major parts, assemblies, and sub-assemblies become available, or are determined, these will be included in this section of subsequent Quarterly Reports.

B. Processes and Processing

1. General

The tentative Process Flow Chart for the TA-2167 is shown in Figure 5. These processes are those which presently appear to be best suited to produce this type of device in the required quantities. As processes are modified, and equipment developed and put into operation, the changes will be reported in this section of subsequent Quarterly Reports. As the specific processes are optimized and standardized, these standards will be reported. The general methods used to fabricate the TA-2167 are those applicable to a triple-diffused silicon mesa device.

2. Diffusion

The impurity profile of a transistor suitable for high-voltage applications is shown in Figure 6. The surface concentration of the base region (C_1) is approximately an order of magnitude lower than the emitter region. This determines the emitter breakdown voltage. A simple double-diffused structure has a inherently high collector spreading resistance. This condition leads to a higher saturation resistance than exhibited by a single diffused device. Therefore, another N-type layer is

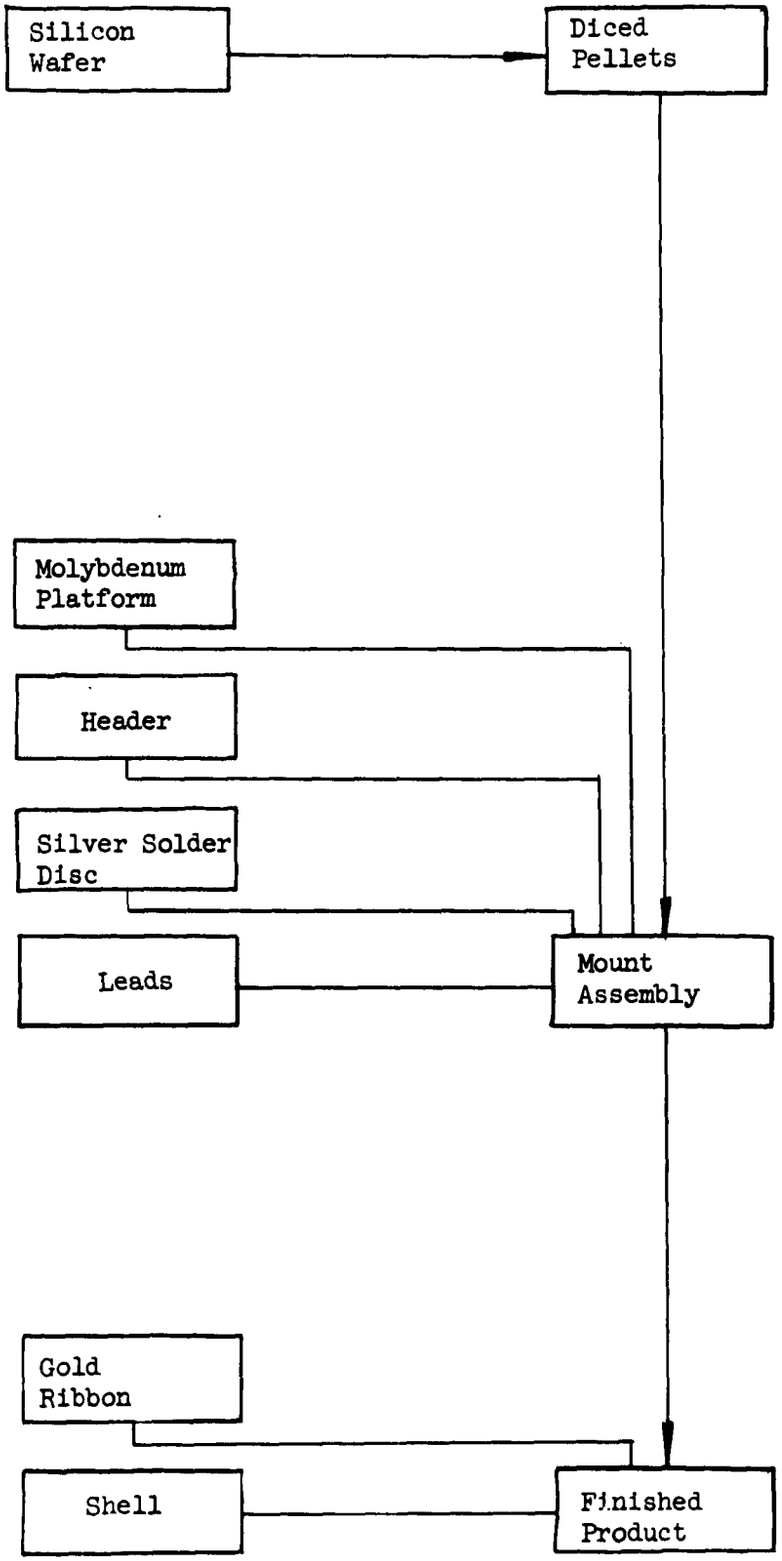


FIGURE 4

PARTS AND MATERIALS FLOW CHART FOR TA-2167 TYPE TRANSISTOR

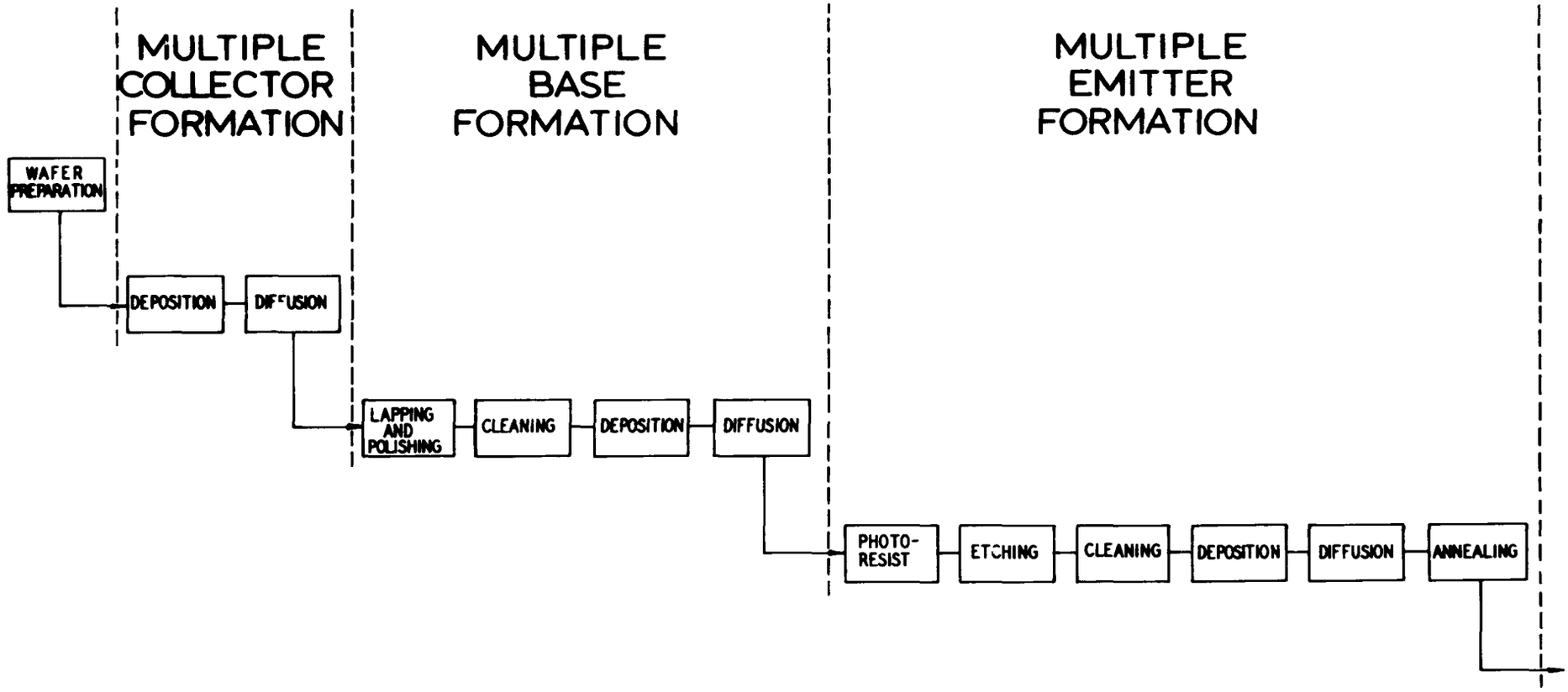


FIGURE 5

A FLOW CHART OF PRESENT PROCESSING FOR THE TA-2167
SILICON POWER TRANSISTOR

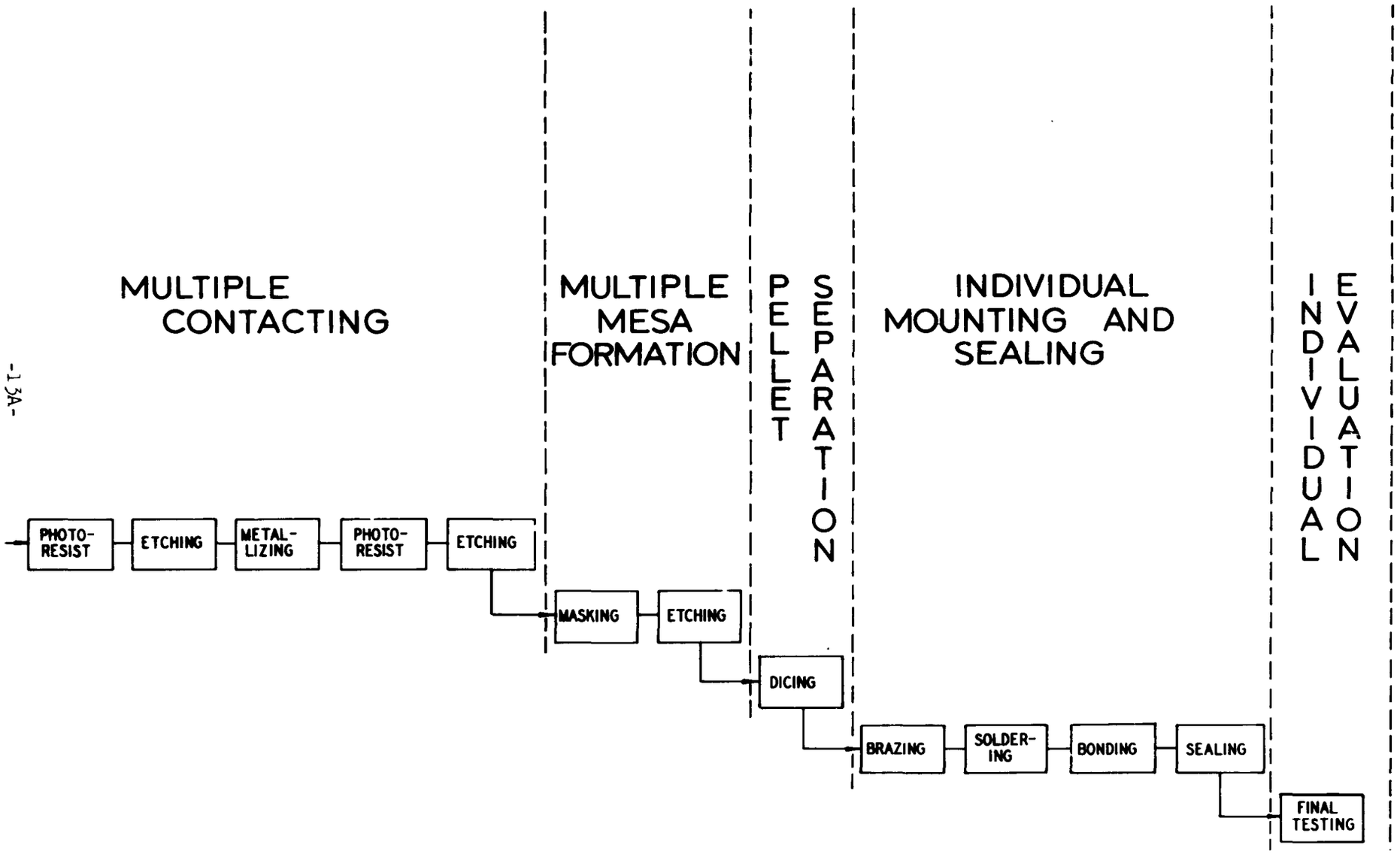


FIGURE 5A

cont'd

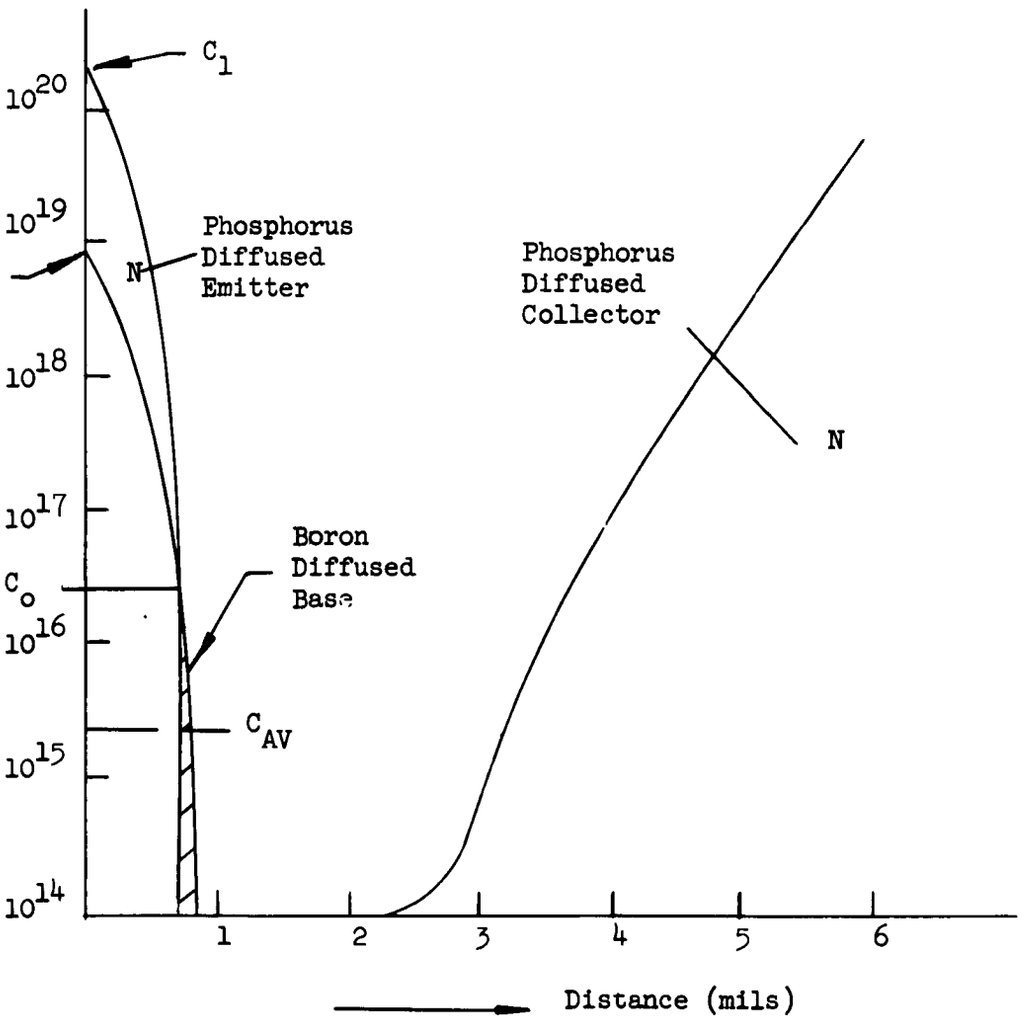


FIGURE 6

IMPURITY PROFILE FOR HIGH VOLTAGE SILICON TRANSISTORS

shown on the right side of the figure. This collector diffusion reduces the collector spreading resistance and results in the final NPIN structure.

Several diffusion runs have been started in the Model Shop. These runs are for the purpose of training operators, "debugging" the equipment, and determining possible production problems.

3. Collector Formation

Only preliminary work has been done in this area.

4. Base Formation

Only preliminary work has been done in this area.

5. Emitter Formation

Some work has been done in this area. The present photographic plates permit only four units per wafer to be formed. It was felt that this was insufficient for production quantities. As a result, the photographic plates have been redesigned to increase the number of units per wafer. These redesigned plates will necessitate changes in handling equipment in order to realize the maximum benefit from the change. This work is beginning.

6. Contacting

Only preliminary work has been done in this area.

7. Mesa Formation

Only preliminary work has been done in this area.

8. Dicing

Only preliminary work has been done in this area.

9. Mounting and Sealing

The use of a molybdenum platform, located between the header and

the pellet, has been initiated. The thickness is to be 0.050" and will permit the required brazing operation without introducing problems of warping during subsequent operations. The noble metal braze used to place the molybdenum platform on the header eliminates the need to use a lead solder and thus permits higher temperature operation. Relatively simple fixtures have been designed to accurately locate the platform on the header during brazing. Figure 7 is a photograph of a device showing the 0.050" molybdenum platform located on the header.

The connector leads which are used on this device are made of 0.005" x 0.020" gold ribbon. This ribbon has been found superior to the previous wire because the thermocompression bonding operation is simplified and produces a resultant reduction in fabrication time and improvement in the quality of the bonds. It has also been found that this lead material will conduct up to 25 amperes of current thus allowing a good margin of safety for the 10 amperes required for this device. Figure 8 is a photograph of a device with the gold ribbon leads.

FIGURE 7

PHOTOGRAPH OF A DEVICE SHOWING THE 0.050" MOLYBDENUM PLATFORM LOCATED ON THE HEADER

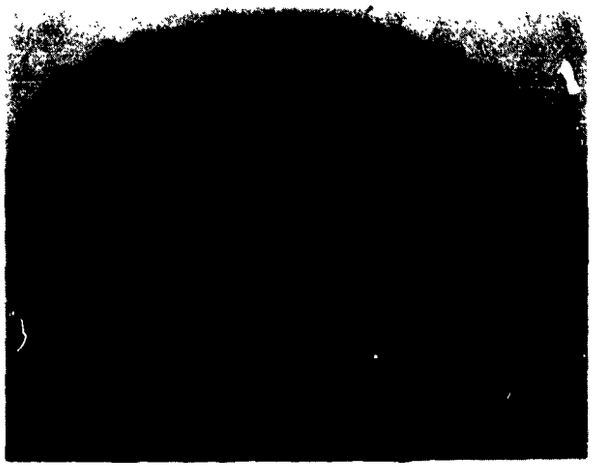


FIGURE 8

PHOTOGRAPH OF A UNIT BONDED USING THE TWO GOLD RIBBONS

IV. DEVICE EVALUATION

A. Electrical

Five state-of-the-art samples were given to Mr. C. Fisher of the Signal Corps on September 22, 1961. The electrical characteristics of these samples are tabulated in Table I.

	I_{CBO} § at 400 V	I_{CEO} at 300 V	I_{EBO} at 8 V	h_{FE} 0.1 A 0.5 V	h_{FE} 1 A 10 V	h_{FE} 5 A 10 V	h_{FE} 10 A 4 V	V_{CE}(sat) 0.5 A 5 A	Crossover Voltage at 1A with 4.20 pulse	C_{ob} μμf
138-9	0.7	0.6	0.16	25	45	58	12.5	0.20	100	182
138-5	0.4	0.15	0.8	50	111	110	12.0	0.27	90	201
135-2	4.0	4.0	0.3	50	59	63	12.0	0.22	90	165
135-5	1.4	1.0	0.002	20	56	56	10.0	0.25	90	171
135-6	0.01	0.01	3.2	9	56	63	12.5	0.20	90	136
§ All current readings in ma										

TABLE I

ELECTRICAL CHARACTERISTICS OF INITIAL FIVE STATE-OF-THE-ART SAMPLES

Experiments on contact resistance have been performed in our laboratory. Results as low as 0.25 °C/watt, with silicone grease applied between the mating surfaces, have been obtained. An efficient heat sink, whose thermal resistance is in the neighborhood of 0.2 °C/watt, may be obtained by using the water-cooled method. Since Θ_{CA} is the sum of the contact and heat sink thermal resistances, in this case Θ_{CA}=0.25+ 0.2=0.45°C/W, there seems to be some inconsistency between this value and that specified in the detailed operating life requirements for this contract. Work to resolve this apparent inconsistency is continuing.

B. Environmental

Only preliminary work has been done in this area.

V. CONCLUSIONS

It is now possible to make, in the laboratory, devices which satisfy the end requirements for circuitry. However, some development work is required before the model shop and pilot line are able to fabricate devices which can satisfy the full contract reliability specifications for operating life, mechanical, and environmental tests.

A double-ended stud package has been proven feasible from a design point of view.

Improvements in the mounting and bonding area have made the fabricated devices more rugged.

VI. PROGRAM FOR NEXT QUARTER

During the next quarter, the following work should be completed:

1. Evaluate the double-ended stud package regarding thermal resistance, quality of seal obtainable etc.;

2. Expand the Model Shop pilot line capability;

3. Improve the device yield to the high-current, high-voltage requirement;

4. Design jigs and fixtures for use in mechanical and environmental tests;

5. Establish an operating point for the Operating Life Test. This will depend upon the case-to-ambient allowance as determined by the Contracting Agency and RCA.

VII. PERSONNEL AND MAN HOURS

The biographies of the personnel contributing directly to this program are listed below. Table II is a tabulation of the Man Hours expended on this contract during the First Quarter.

KEITH E. LOOFBOURROW - Manager, Industrial Transistor Product Development

Mr. Loofbourrow received the BSEE degree from Oklahoma State University in 1950. He joined RCA as an Engineering Trainee after college. He gained extensive knowledge and experience in receiving tubes and transistors during the next five years as an application engineer and later as an engineering leader. He was then promoted to Manager, Test Engineering for the Semiconductor Division and served in that capacity until 1957 when he was promoted to the position of Manager, Industrial Application Engineering for the Semiconductor Division. Mr. Loofbourrow was promoted to his present position in 1961, and the work done under this contract will be administered by him.

Mr. Loofbourrow has published extensively in various journals on the design and application of various tubes and transistors.

GERALD J. ANDESKIE - Manager, High-Frequency Silicon Model Shop

Mr. Andeskie received the B.S. degree in Engineering Administration from Rutgers University. He joined the RCA Semiconductor Division in October, 1956 as Engineering Administrator to the Chief Engineer. He assumed his present position on January 1, 1959. Prior to coming with RCA, Mr. Andeskie served two years with the U. S. Air Force as Aircraft Maintenance Engineering Officer and Production Control Officer. He also spent two years with the U. S. Gypsum Company as Project Engineer.

ZUNG F. CHANG

Mr. Chang was born in Shanghai, China and came to this country where he graduated from Rensselaer Polytechnic Institute in 1959 with a BEE degree. He

joined the RCA Semiconductor and Materials Division in 1959 as an Engineering Trainee. Following his training he joined the Industrial Device Applications Group as an application engineer. Mr. Chang will be doing much of the circuitry work associated with this contract.

HERBERT R. MEISEL

Mr. Meisel received the B.M.E. degree from Rensselaer Institute in 1950. He received the MS degree in Management Engineering from Newark College of Engineering in 1956 and the MS degree in Physics from Stevens Institute of Technology in 1958. Mr. Meisel joined the RCA Semiconductor Division in 1953 as a design and development engineer. His projects have included: germanium alloy audio and power transistors, alloyed silicon rectifiers, Signal Corps micromodule transistors, Signal Corps Device 1 PNP germanium, and Devices 13, 14 and 15 NPN and PNP diffused silicon transistors. These projects have included extensive experience in industrial preparedness studies. Prior to joining RCA, Mr. Meisel was an Ordiance Test Engineer at Aberdeen Proving Grounds, Maryland and a Student Electronics Officer in the U. S. Air Force. Mr. Meisel assumed his present duties as Group Leader in October, 1960.

SEYMOUR SILVERSTEIN

Mr. Silverstein received the B.M.E.degree from City College of New York in 1951 and the B.E.E. degree from the same college in 1956. Mr. Silverstein joined RCA as a Trainee in 1951 and worked in the Tube Division at Harrison, Lancaster and Camden. Following his Trainee time he was assigned to Camden where he worked on broadcast TV antennas as a design engineer. He joined the Semiconductor Division and was assigned to the Development Shop in Harrison in 1951 and later transferred to Somerville with this organization. During this time he developed, refined, and optimized the processes for devices prior to having them transferred to the factory. In 1959 he was transferred to the Semiconductor Model Shop where

he gained extensive knowledge about Pilot Production of devices. While there Mr. Silverstein was also instrumental in training operators for the various processes. In 1961 he was promoted to design engineering and assigned to the Industrial Design group of the Semiconductor Division. Since that time he has been responsible for the design and prototype work on several devices. Mr. Silverstein is now a Senior Engineer with RCA.

Mr. Silverstein holds one patent for "Jig Alloying of Semiconductor Devices" (Patent No. Z, 964, 431).

NORMAN C. TURNER

Mr. Turner received the B.S. degree in Mechanical Engineering from Rutgers University in 1958. Prior to attending Rutgers, he was employed by the Service Machine Co. as a tool and die maker and also did some tool and machine design work. Following his graduation from Rutgers he was a rocket engine project engineer with the Reaction Motors Division of Thiokol Chemical Co. Mr. Turner was an Ordiance Mechanical Engineering Officer in the U. S. Army from 1958 to 1959. He joined RCA in December, 1959 and has been assigned to the Industrial Model Shop since that time.

JEROME E. WRIGHT

Mr. Wright attended Wilkes College from 1952 to 1954, and received the B.S.E.E. degree from Pennsylvania State University in 1956. He joined RCA in June, 1956 as a Trainee in the Training Program. Mr. Wright joined the Semiconductor Division section as a device engineer. His projects have included: germanium alloy audio and power transistors, Signal Corps Device 1 PNP and NPN germanium transistors, low and high power germanium transistors, and the triple diffused silicon high frequency lifetest program. Mr. Wright has had extensive experience in industrial preparedness studies programs.

	June	July	August	September	Total
S. Silverstein		27	40	68	135
H. Meisel		36	61	45	142
J. Wright		30	48	30	108
J. Molnar		-	20	1	21
M. Tutle			4	-	4
	No Time Recorded	93	173	144	410
Misc.		16	50	8	74
		-	3	-	3
		109	226	152	487

TABLE II

MAN HOURS FOR THE FIRST QUARTER